dielectric material formed on the substrate surface and wherein the trench defines the distance between the device source and the device drain.

2. (unchanged) The semiconductor device of claim 1 wherein the distance between the spacers defines a device gate length.

3. (unchanged) The semiconductor device of claim 2 wherein the distance between the spacers is less than 50 nm.

REMARKS

This reply is in response to the Official Action mailed May 31, 2001. The Examiner made that Official Action FINAL.

In that Official Action, the Examiner rejected applicants' claims 1 and 2 under 35 USC § 102(b). The Examiner cited U.S. Patent No. 6,090,672 to Wanlass (Wanlass hereinafter) as the basis for the rejection.

As noted by the applicants, one of the problems with prior art sacrificial gates was the fact that the sacrificial gate itself was the fact that the sacrificial gate itself defines the distance between the source and the drain. This is readily observed in FIG. 5C of Wanlass. In Wanlass, the spacer defines the distance between the source and drain and subsequently the width of trench 12. The device gate is formed in the trench.

Wanlass clearly does not describe a device in which the device gate and spacers are formed in a trench and the device gate is interposed between the spacers. Wanlass is therefore clearly contrary to applicants' invention. Claim 1 is amended to expressly recite that the gate is interposed between the spacers. In Wanlass the spacer 9 is removed from the trench before the gate is formed therein. See column 4 lines 3-9 of Wanlass and the accompanying drawings.

To summarize, Wanlass uses a single spacer (FIG. 6A to 7B) to define the device gate length. See column 3, lines 46-49 ("A thin layer 9 of amorphous silicon ~ 50 nm thick is conformally deposited, as shown in FIG. 4C. The thickness of layer 9 will determine the channel length of the final MOS transistor") (emphasis added).

The difference between the device described in Wanlass and the device claimed by applicants, is readily observed with reference to FIG. 7 in applicants' specification. Specifically, the gate dielectric 140 and polycrystalline gate 141 is interposed between spacers 135. Claim 1 is amended to specifically recite that the gate is interposed between the spacers. Both the gate and the spacers are formed in the trench. The advantages of using the replacement gate and spacers to define the distance between the source and drain of the device is described on page 3, lines 4 to 28 of applicants' specification. Specifically, since the trench width is the combined gate length and spacer width, the lithographic requirements for defining the gate length are relaxed.

Wanlass does not disclose or suggest a device in which both spacers and gate are formed in a trench with the distance between the spacers defining the gate length. In Wanlass, the spacer is a sacrificial spacer used to define the width of the trench. After the spacer is removed, it is replaced by a gate formed in the trench. Thus, in Wanlass, the gate length and the distance between the source and drain are the same. This result does not obtain from applicants' invention. Specifically, the distance between the source and drain (i.e. the trench width) is the width of the spacers *plus* the gate length. Since amended claim 1 requires that the gate be interposed between spacers formed in a trench, Wanlass does not anticipate amended claim 1. Nor does Wanlass anticipate claim 2, which, though unamended, is patentable over Wanlass by virtue of its dependence on claim 1.

Nor does Wanlass render obvious applicants' invention under 35 U.S.C. § 103. As noted in applicants' specification, it is difficult to lithographically define device features with dimensions of less than 50 nm. In applicants' device, the

device gate length is not defined lithographically. Instead, the trench width, which includes the gate length and spacer width, is defined lithographically. The sub lithographic gate length is defined by forming both the spacers and the gate in the trench. Wanlass clearly does not disclose or suggest: 1) trench formation; followed by 2) formation of spacers in the trench; followed by 3) formation of a gate between spacers. Thus Wanlass does not render obvious applicants' invention.

The Examiner rejected claim 3 as obvious under 35 U.S.C. § 103(a). The Examiner cited Chatterjee et al. as the basis for this rejection.

Claim 3 depends from amended claim 1. Amended claim 1 is patentable over Wanlass for the reasons that were previously stated. Hence claim 3 is patentable by virtue of its dependence from claim 1.

The other references cited, but not relied upon, by the Examiner were considered by the applicants but not deemed pertinent to this discussion.

For the foregoing reasons, applicants submit that their amended claims are in condition for allowance. Favorable action from the Examiner is respectfully requested.

Any official fees associated with the entry and consideration of this Amendment may be charged to **Agere Systems Inc.** Deposit Account 501735.

Respectfully submitted,

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MARKED-UP VERSION OF AMENDED CLAIMS

1. (amended) A semiconductor device comprising:

a semiconductor substrate in which a source, drain and channel are formed;

a gate formed on a gate dielectric layer formed on the semiconductor substrate;

spacers adjacent to the gate wherein the gate is interposed between the spacers and the gate and spacers are formed in a trench formed in a layer of dielectric material formed on the substrate surface and wherein the trench defines the distance between the device source and the device drain.

2. (unchanged) The semiconductor device of claim 1 wherein the distance between the spacers defines a device gate length.

3. (unchanged) The semiconductor device of claim 2 wherein the distance between the spacers is less than 50 nm.